

Sup/IRBuck™

USER GUIDE FOR IR3843W EVALUATION BOARD

DESCRIPTION

The IR3843W is a synchronous buck converter, providing a compact, high performance and flexible solution in a small 5mmx6mm Power QFN package.

Key features offered by the IR3843W include programmable soft-start ramp, precision 0.7V reference voltage, Power Good, thermal protection, programmable switching frequency, Sequence input, Enable input, input under-voltage lockout for proper start-up, and pre-bias start-up.

An output over-current protection function is implemented by sensing the voltage developed across the on-resistance of the synchronous rectifier MOSFET for optimum cost and performance.

This user guide contains the schematic and bill of materials for the IR3843W evaluation board. The guide describes operation and use of the evaluation board itself. Detailed application information for IR3843W is available in the IR3843W data sheet.

BOARD FEATURES

- $V_{in} = +12V$ (13.2V Max)
- $V_{cc} = +5V$ (5.5V Max)
- $V_{out} = +1.8V @ 0- 2A$
- $F_s = 600kHz$
- $L = 3.3\mu H$
- $C_{in} = 1 \times 10\mu F$ (ceramic 1206) + $330\mu F$ (electrolytic)
- $C_{out} = 2 \times 22\mu F$ (ceramic 0805)

CONNECTIONS and OPERATING INSTRUCTIONS

A well regulated +12V input supply should be connected to VIN+ and VIN-. A maximum 2A load should be connected to VOUT+ and VOUT-. The connection diagram is shown in Fig. 1 and inputs and outputs of the board are listed in Table I.

IR3843W has two input supplies, one for biasing (Vcc) and the other as input voltage (Vin). Separate supplies should be applied to these inputs. Vcc input should be a well regulated 4.5V-5.5V supply and it would be connected to Vcc+ and Vcc-.

If single 12V application is required connect R7 (zero Ohm resistor) which enables the on board bias regulator (see schematic). In this case there is no need of external Vcc supply.

The output can track a sequencing input at the start-up. *For sequencing application, R16 should be removed and the external sequencing source should be applied between Seq. and Agnd.* The value of R14 and R28 can be selected to provide the desired ratio between the output voltage and the tracking input. *For proper operation of IR3843W, the voltage at Seq. pin should not exceed Vcc.*

Table I. Connections

Connection	Signal Name
VIN+	V _{in} (+12V)
VIN-	Ground of V _{in}
Vcc+	Vcc input
Vcc-	Ground for Vcc input
VOUT-	Ground of V _{out}
VOUT+	V _{out} (+1.8V)
Enable	Enable
Seq.	Sequence Input
P_Good	Power Good Signal

LAYOUT

The PCB is a 4-layer board. All of layers are 2 Oz. copper. The IR3843W SupIRBuck and all of the passive components are mounted on the top side of the board.

Power supply decoupling capacitors, the Bootstrap capacitor and feedback components are located close to IR3843W. The feedback resistors are connected to the output voltage at the point of regulation and are located close to the SupIRBuck. To improve efficiency, the circuit board is designed to minimize the length of the on-board power ground current path.

Connection Diagram

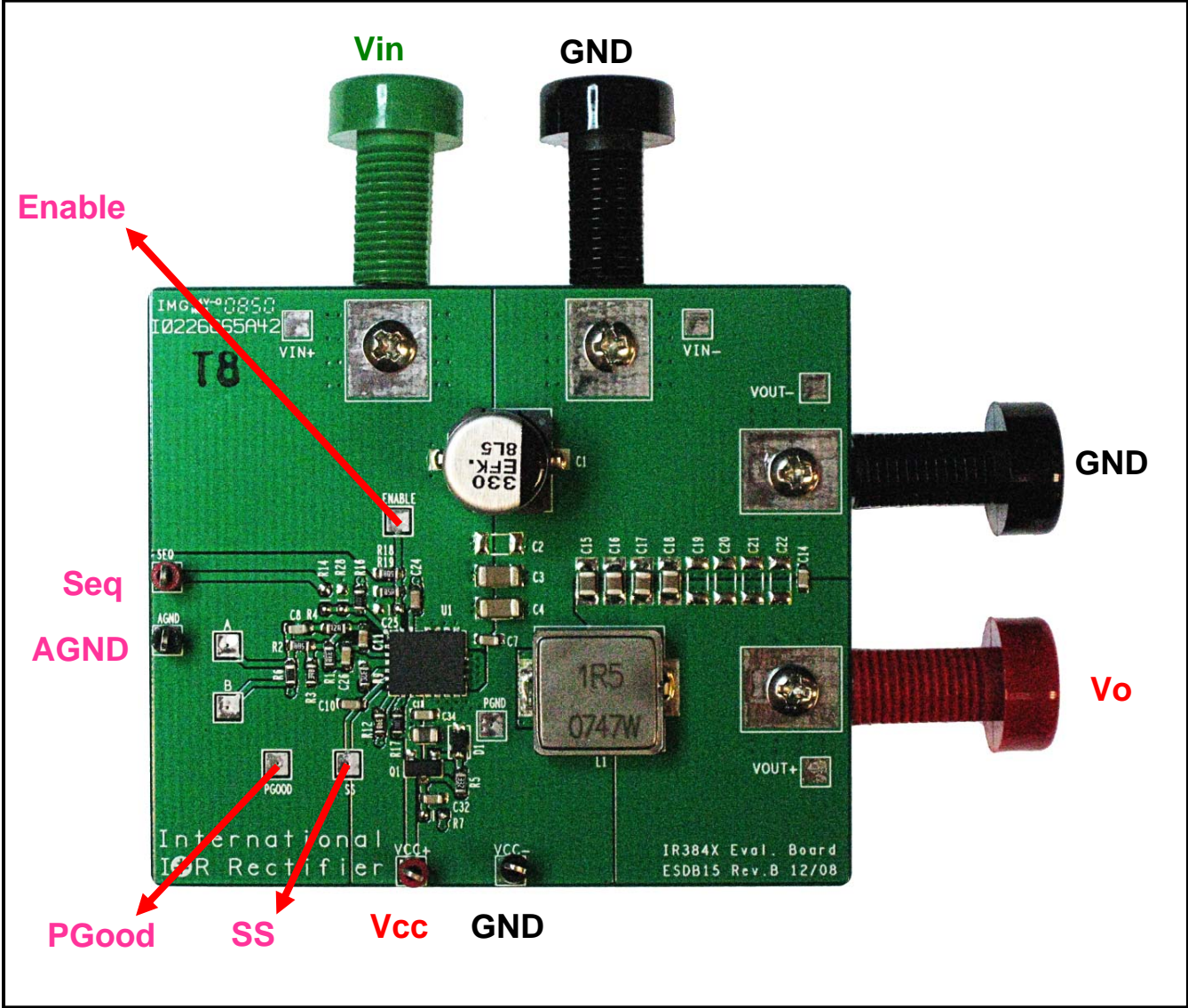


Fig. 1: Connection diagram of IR384xW evaluation boards

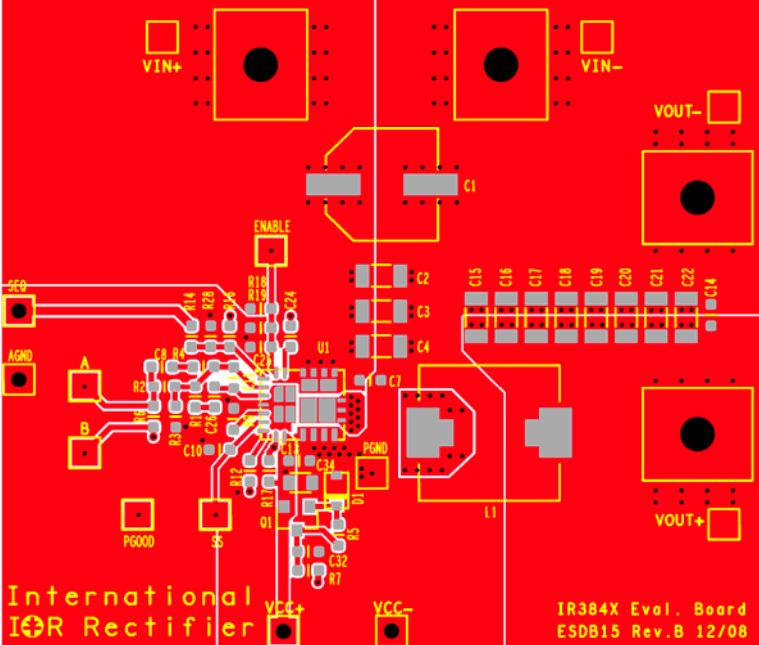


Fig. 2: Board layout, top overlay

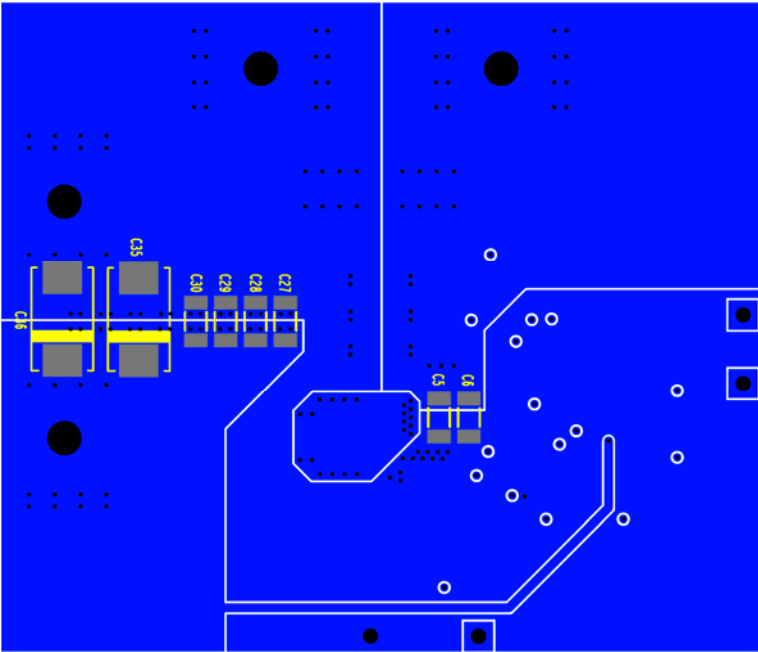


Fig. 3: Board layout, bottom overlay (rear view)

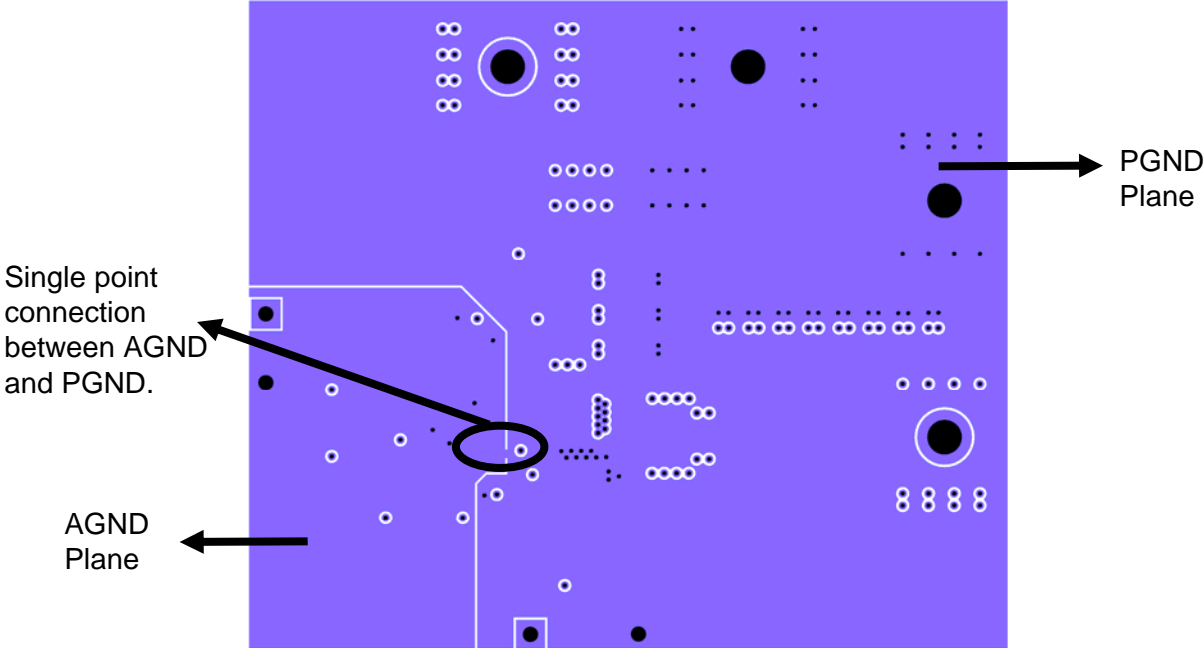


Fig. 4: Board layout, mid-layer I.

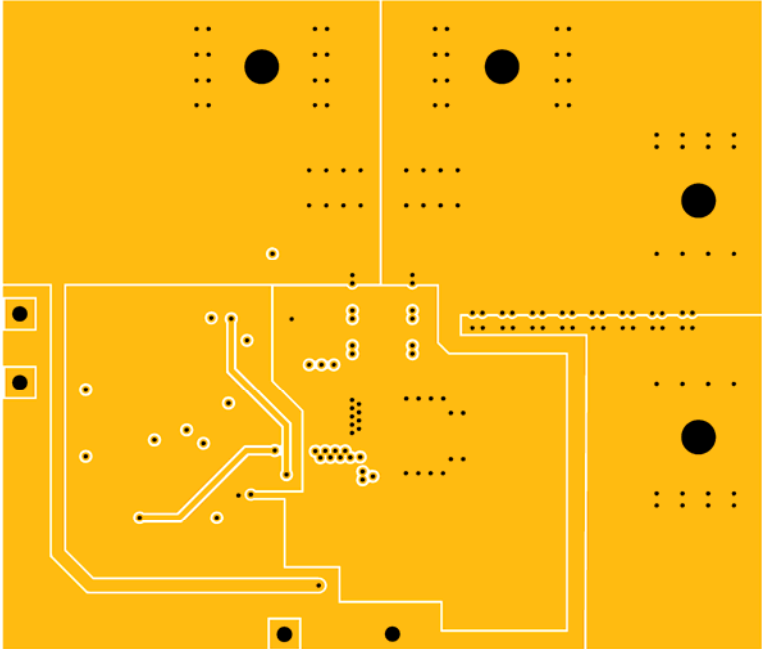
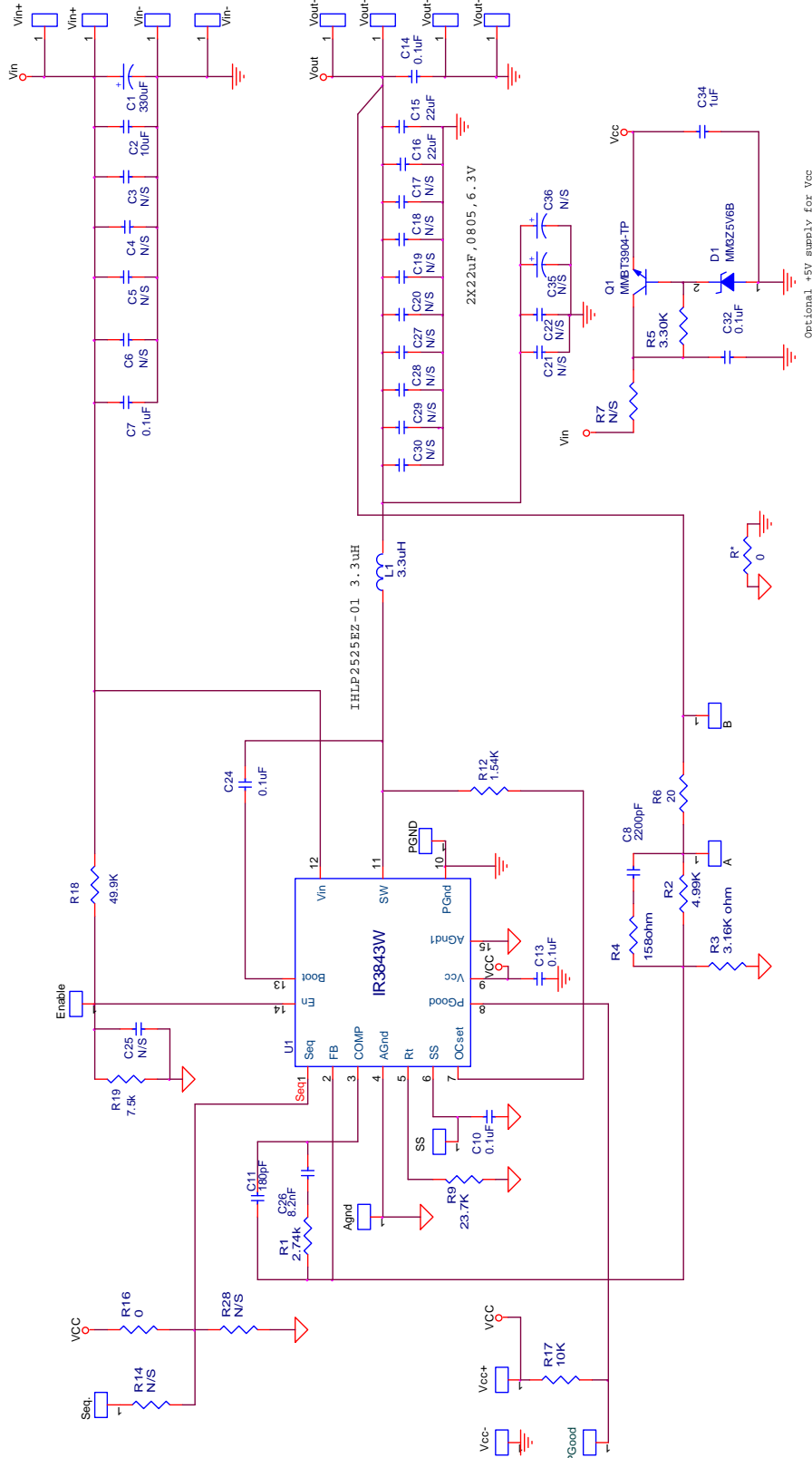


Fig. 5: Board layout, mid-layer II.



Single point of connection between Power
Ground and Signal ("analog") Ground

Fig. 6: Schematic of the IR3843W evaluation board

Bill of Materials

Item	Quantity	Part Reference	Value	Description	Manufacturer	Part Number
1	1	C2	10uF	1206,16V, X7R, 20%	Panasonic - ECG	ECJ-3YX1C106K
2	1	C1	330uF	SMD Electrolytic, Fsize, 25V, 20%	Panasonic	EEV-FK1E331P
3	6	C7 C14 C24 C10 C13 C32	0.1uF	0603, 25V, X7R, 10%	Panasonic	ECJ-1VB1E104K
4	1	C8	2200pF	2200pF,0603,50V,X7R	Panasonic	ECJ-1VB1H222K
5	1	C11	180pF	50V, 0603, NP0, 5%	Panasonic	ECJ-1VC1H181J
6	2	C15 C16	22uF	0805, 6.3V, X5R, 20%	Panasonic	ECJ-2FB0J226M
7	1	C26	8200pF	0603, 50V, X7R, 10%	Panasonic	ECJ-1VB1H822K
8	1	L1	3.3uH	6.9x6.5x5mm, 8A,20%	Vishay/Dale	IHLP2525EZ-01 3.3uH
9	1	R1	2.74k	0603,1/10W,1%	Rohm	MCR03EZPFX2741
10	1	R2	4.99k	0603,1/10W,1%	Rohm	MCR03EZPFX4991
11	1	R3	3.16k	0603,1/10W,1%	Rohm	MCR03EZPFX3161
12	1	R4	158	0603,1/10W,1%	Panasonic	ERJ-3EKF1580V
13	1	R6	20	0603,1/10 W,1%	Vishay/Dale	CRCW060320R0FKEA
14	1	R9	23.7K	0603,1/10W,1%	Rohm	MCR03EZPFX2372
15	1	R16	0	0603,1/10 W,5%	Vishay/Dale	CRCW06030000Z0EA
16	1	R12	1.54K	0603,1/10 W,1%	Rohm	MCR03EZPFX1541
17	1	R17	10K	0603,1/10 W,1%	Rohm	MCR03EZPFX1002
18	1	R18	49.9k	0603,1/10 W,1%	Rohm	MCR03EZPFX4992
19	1	R19	7.5k	0603,1/10W,1%	Rohm	MCR03EZPFX7501
20	1	R5	3.3k	0603,1/10W,1%	Rohm	MCR03EZPFX3301
21	1	C34	1uF	1uF, 10V, X5R,0805	Panasonic	ECJ-2FB1C105K
22	1	D1	MM3Z5V6B	Zener,5.6V	Fairchild	MM3Z5V6B
23	1	Q1	MMBT3904/SOT	NPN, 200mA, 40V, SOT23	Fairchild	MMBT3904/SOT
24	1	U1	IR3843W	2A SuplIRBuck. PQFN 5x6mm	International Rectifier	IR3843WMPbF

TYPICAL OPERATING WAVEFORMS

$V_{in}=12.0V$, $V_{cc}=5V$, $V_o=1.8V$, $I_o=0-2A$, Room Temperature, No Air Flow

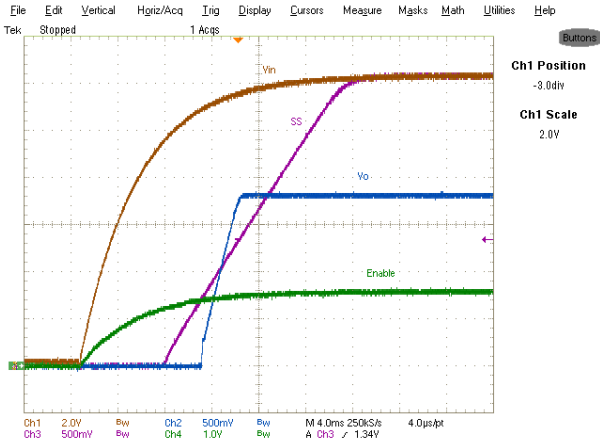


Fig. 17. Start up at 2A Load
Ch₁: V_{in} , Ch₂: V_o , Ch₃: V_{ss} , Ch₄:Enable

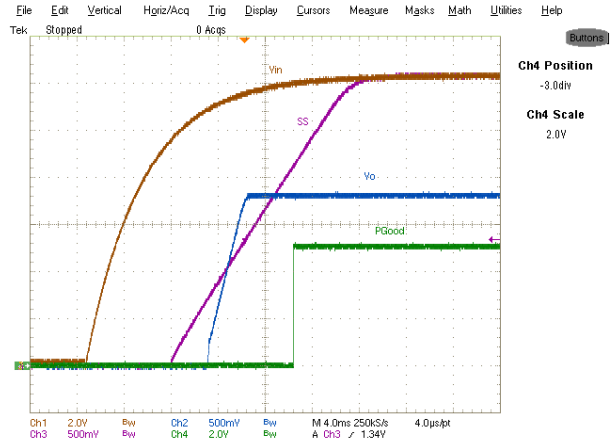


Fig. 18. Start up at 2A Load,
Ch₁: V_{in} , Ch₂: V_o , Ch₃: V_{ss} , Ch₄: V_{PGGood}

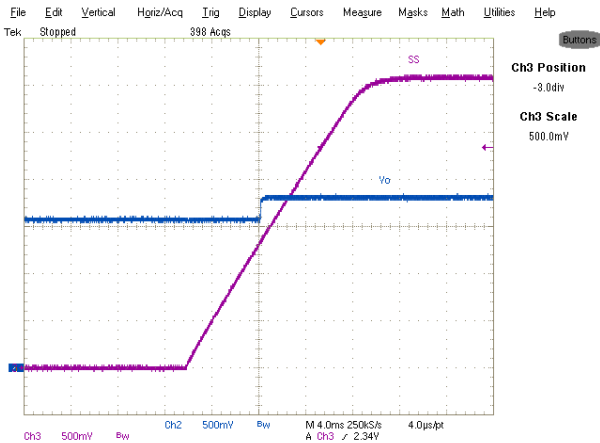


Fig. 19. Start up with 1.62V Pre Bias, 0A Load, Ch₂: V_o , Ch₃: V_{ss}

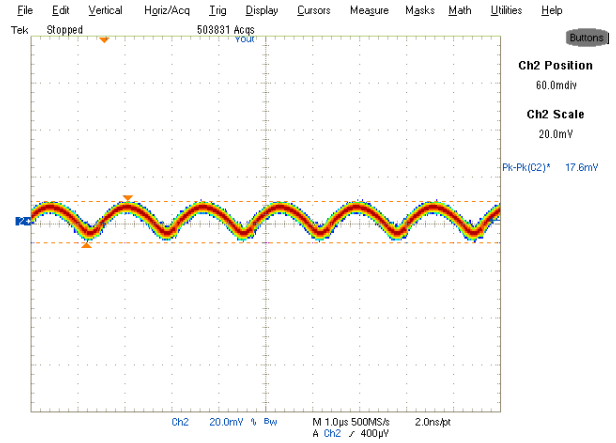


Fig. 20. Output Voltage Ripple, 2A load
Ch₂: V_o

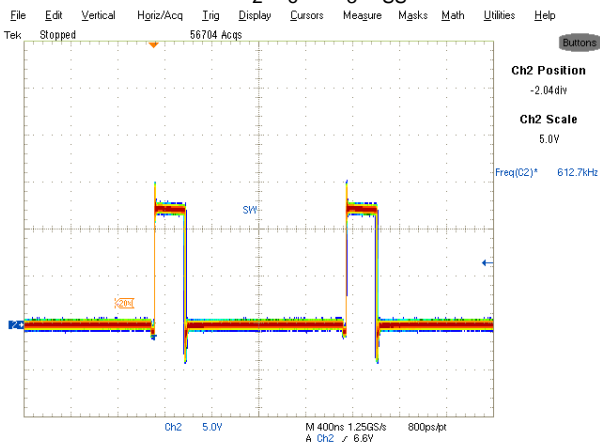


Fig. 21. Inductor node at 2A load
Ch₂:LX

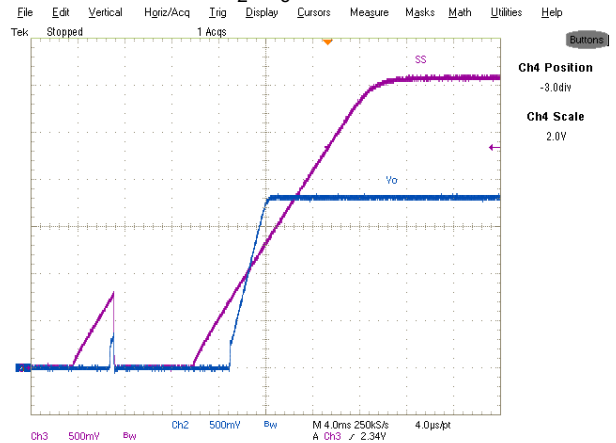


Fig. 22. Short (Hiccup) Recovery
Ch₂: V_o , Ch₃: V_{ss}

TYPICAL OPERATING WAVEFORMS

Vin=12V, Vcc=5V, Vo=1.8V, Io=0-2A, Room Temperature, No Air Flow

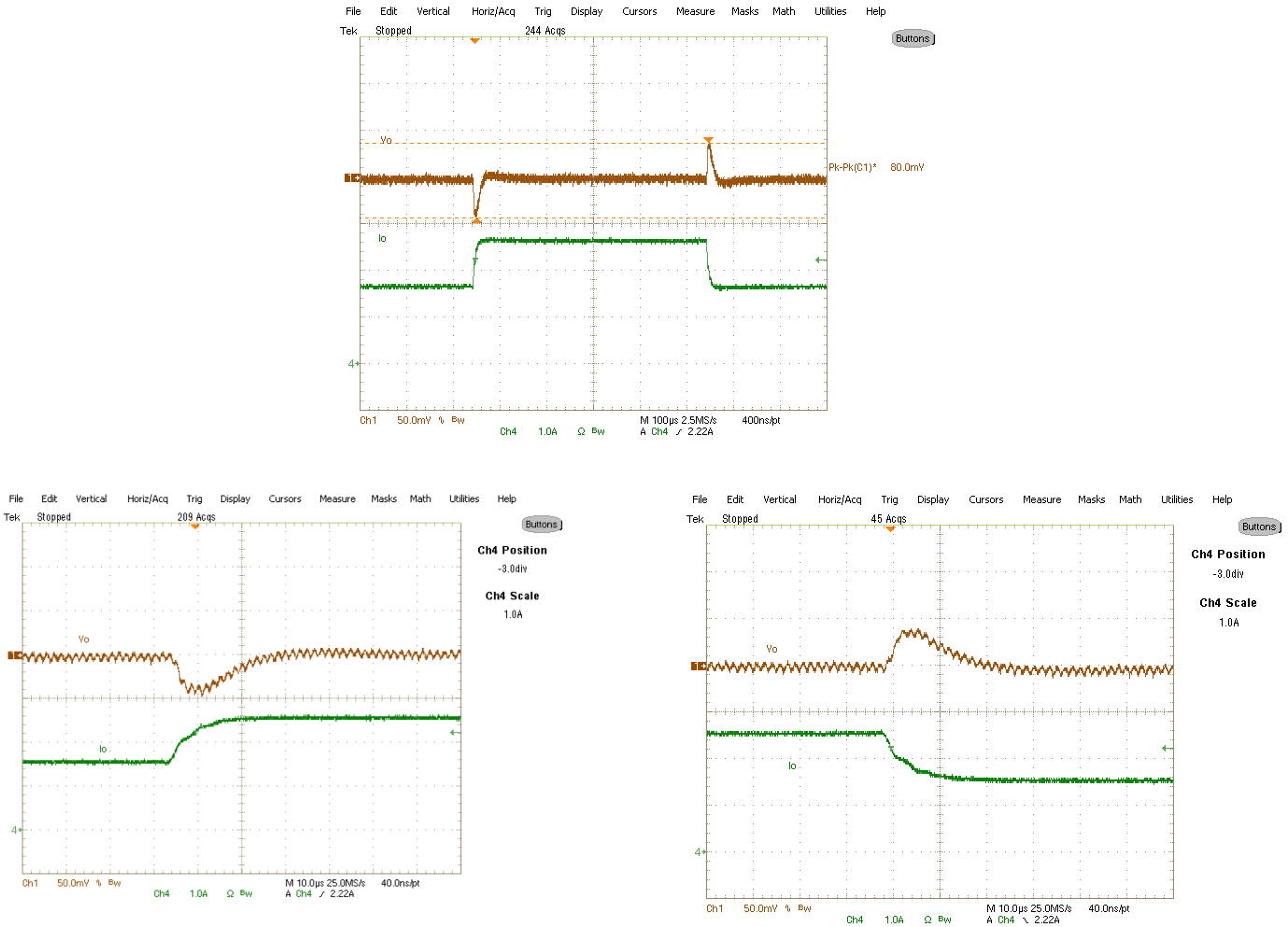


Fig. 23. Transient Response, 1A to 2A step 2.5A/µs
 Ch₁:V_o, Ch₄:I_o

TYPICAL OPERATING WAVEFORMS

Vin=12V, Vcc=5V, Vo=1.8V, Io=2A, Room Temperature, No Air Flow

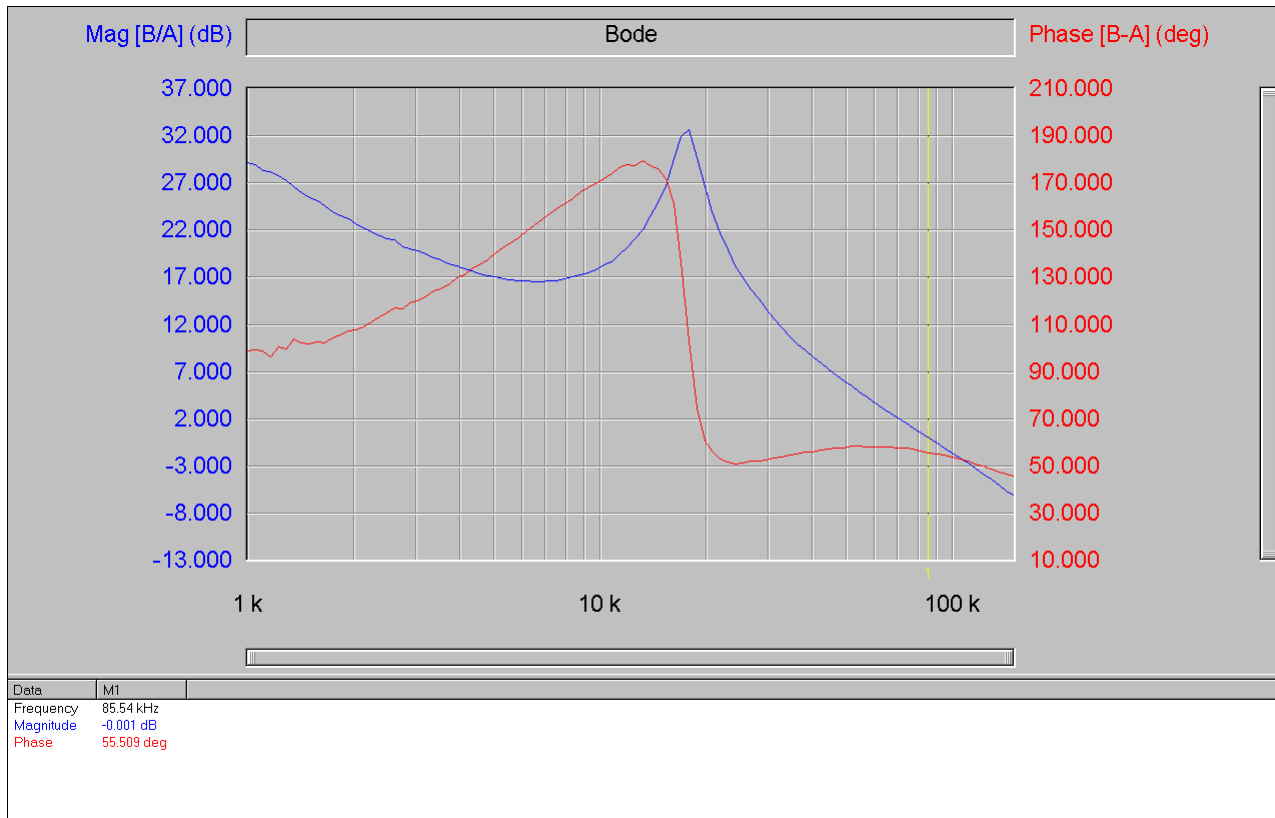


Fig. 24. Bode Plot at 2A load shows a bandwidth of 85.54kHz and phase margin of 55.509 degrees

TYPICAL OPERATING WAVEFORMS
Vin=12V, Vo=1.8V, Io=0- 2A, Room Temperature, No Air Flow

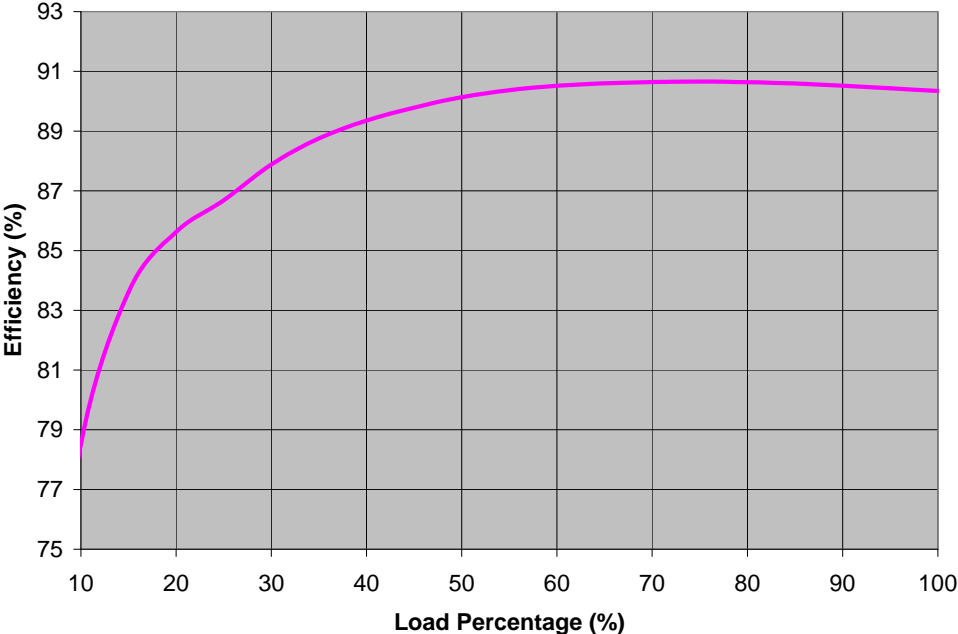


Fig.15: Efficiency versus load current

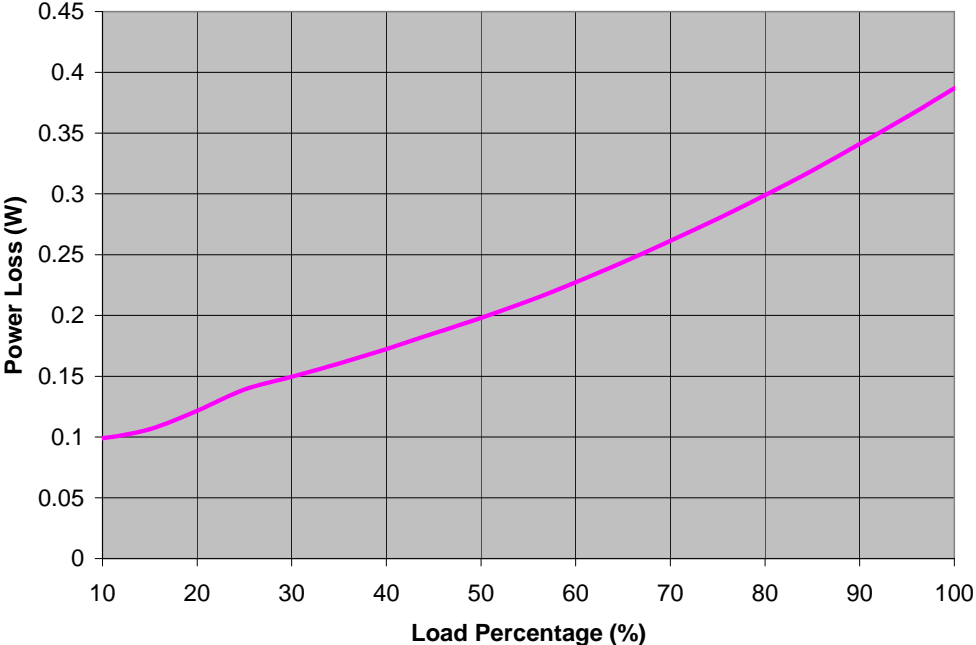


Fig.16: Power loss versus load current

THERMAL IMAGES

Vin=12V, Vo=1.8V, Io=2A, Room Temperature, No Air Flow

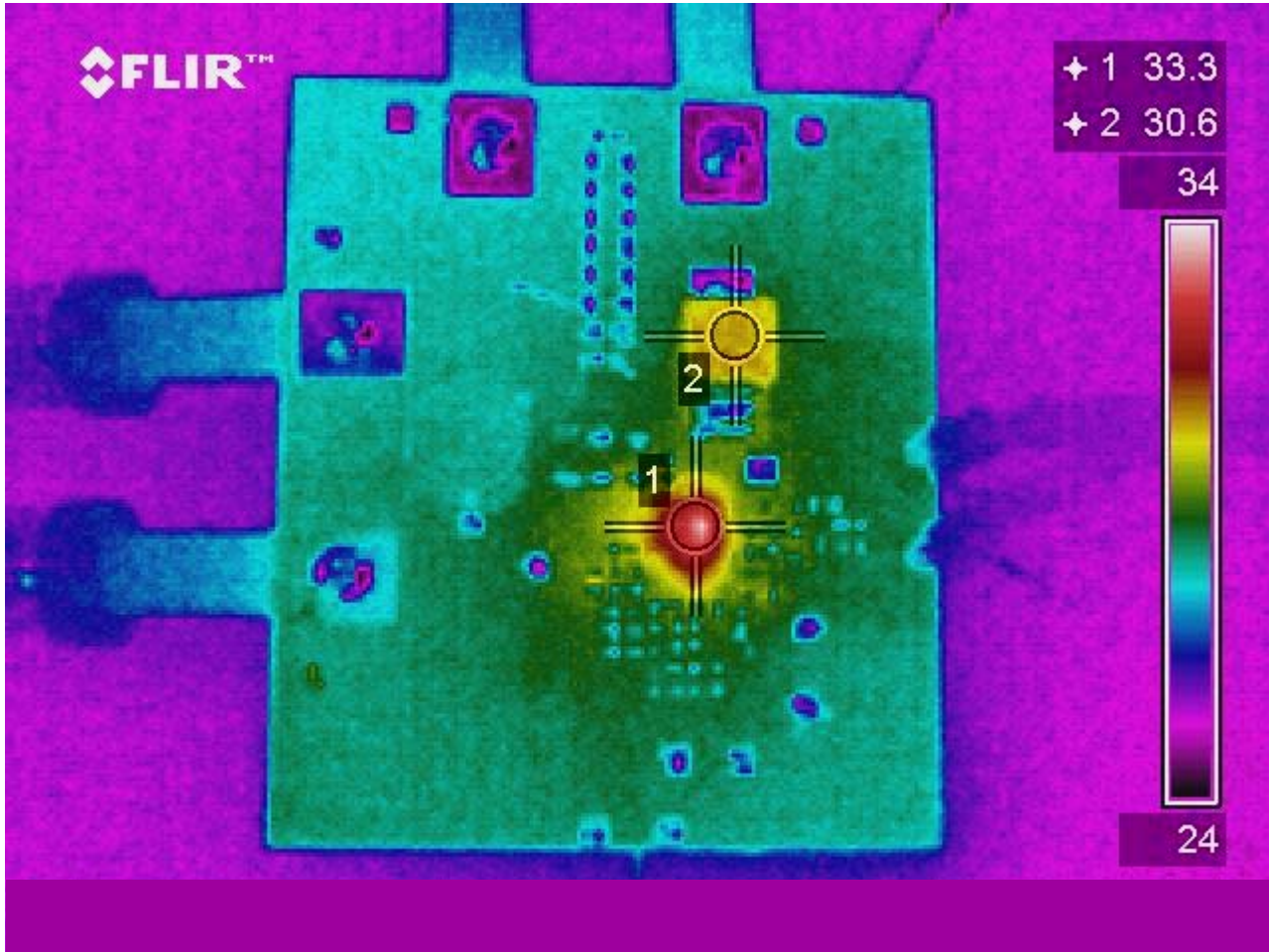


Fig. 17: Thermal Image at 2A load
Test points 1 and 2 are IR3843W and inductor, respectively.

Simultaneous Tracking at Power Up and Power Down
Vin=12V, Vo=1.8V, Io=2A, Room Temperature, No Air Flow

In order to run the IR3843W in the simultaneous tracking mode, the following steps should be taken:

- Remove R16 from the board.
- Set the value of R14 and R28 as R2 (4.99K) and R3 (3.16K), respectively.
- Connect the controlling input across SEQ and AGND test points on the board. This voltage should be at least 1.15 time greater than Vo. For the following test results a 0-3.3V source is applied to SEQ input.
- The controlling input should be applied after the SS pin is clamped to 3.0V.

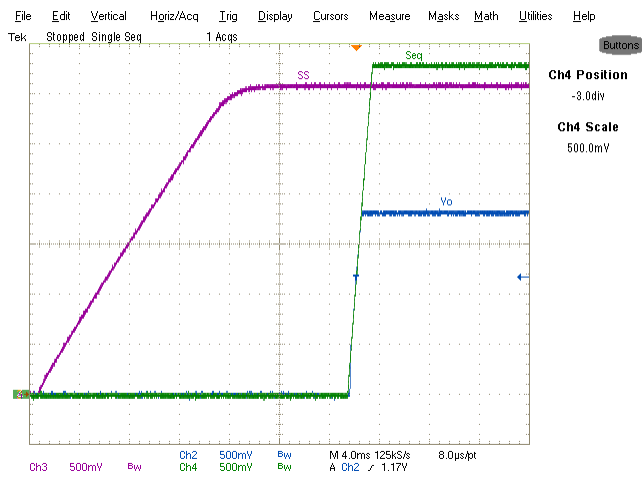


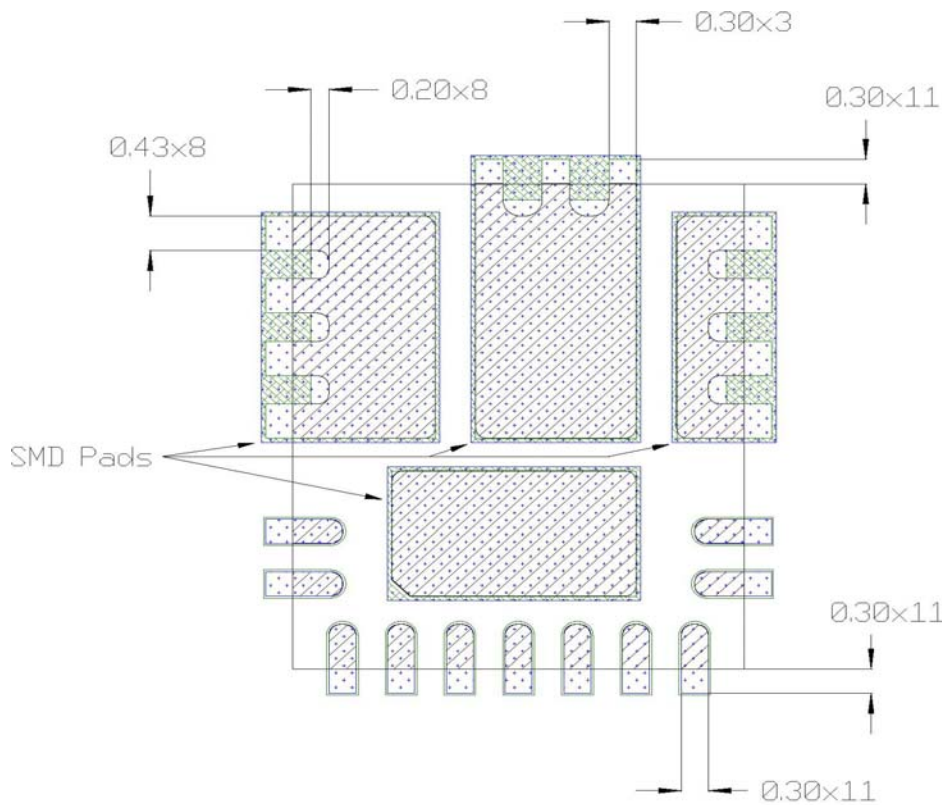
Fig. 18: Simultaneous Tracking a 3.3V input at power-up and shut-down
 Ch2: Vout Ch3:SS Ch4: Seq

PCB Metal and Components Placement

The lead lands (the 11 IC pins) width should be equal to the nominal part lead width. The minimum lead to lead spacing should be $\geq 0.2\text{mm}$ to minimize shorting.

Lead land length should be equal to the maximum part lead length + 0.3 mm outboard extension. The outboard extension ensures a large and inspectable toe fillet.

The pad lands (the 4 big pads other than the 11 IC pins) length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be no less than 0.17mm for 2 oz. Copper; no less than 0.1mm for 1 oz. Copper and no less than 0.23mm for 3 oz. Copper.



All Dimensions in mm

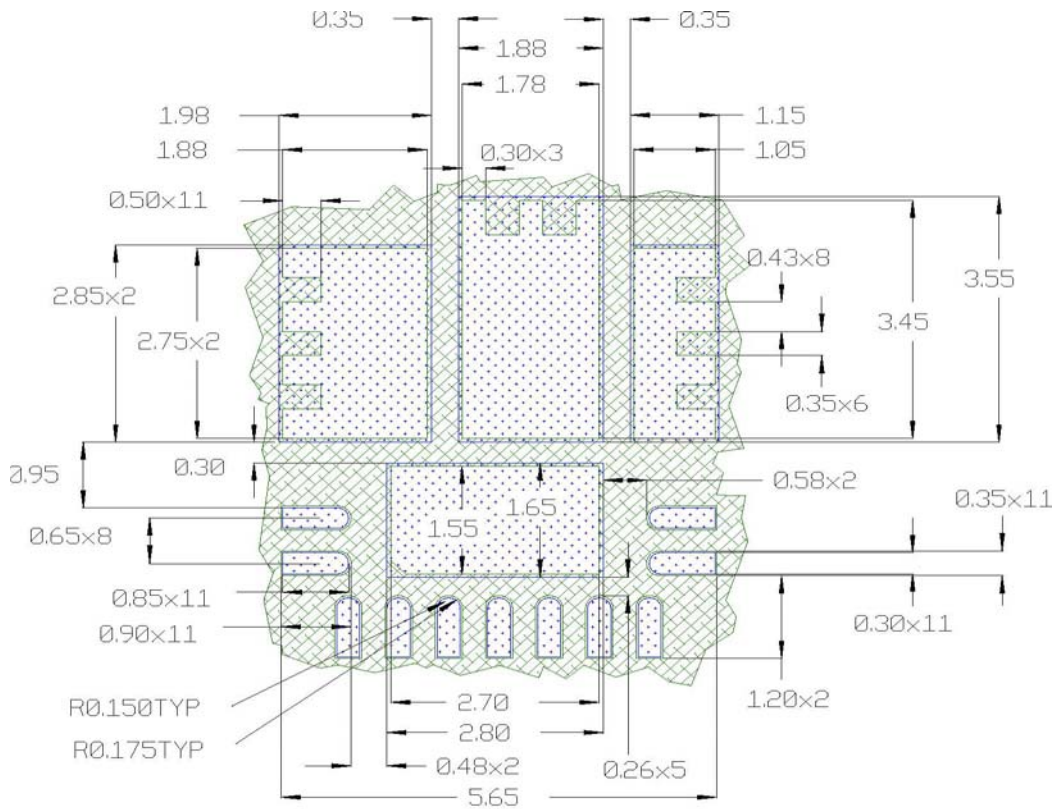
-  PCB Copper
-  Component pad
-  Soldermask

Solder Resist



It is recommended that the lead lands are Non Solder Mask Defined (NSMD). The solder resist should be pulled away from the metal lead lands by a minimum of 0.025mm to ensure NSMD pads.

The land pad should be Solder Mask Defined (SMD), with a minimum overlap of the solder resist onto the copper of 0.05mm to accommodate solder resist mis-alignment.

Ensure that the solder resist in between the lead lands and the pad land is $\geq 0.15\text{mm}$ due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.

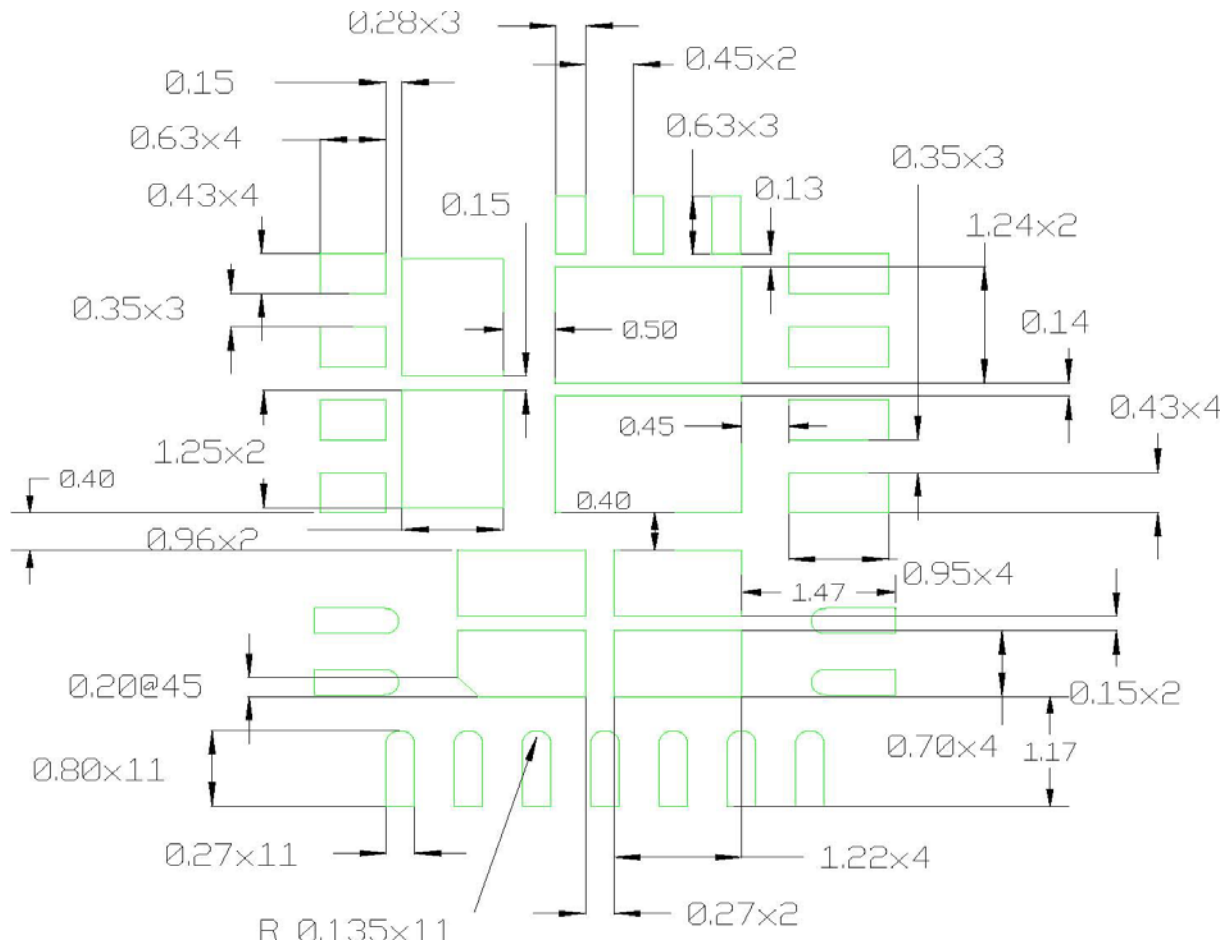


All Dimensions in mm

-  PCB Copper
-  PCB Solder Resist

Stencil Design

- The Stencil apertures for the lead lands should be approximately 80% of the area of the lead lads. Reducing the amount of solder deposited will minimize the occurrences of lead shorts. If too much solder is deposited on the center pad the part will float and the lead lands will be open.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.



Stencil Aperture
 All Dimensions in mm

